Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1055	(711/167).CCLS.	USPAT; USOCR	OR	OFF	2005/11/21 14:18
L2	513	(711/169).CCLS.	USPAT; USOCR	OR	OFF	2005/11/21 14:18
L3	587	(365/230.02).CCLS.	USPAT; USOCR	OR	OFF	2005/11/21 14:18
L4	746	(365/230.05).CCLS.	USPAT; USOCR	OR	OFF	2005/11/21 14:18
L5	20	memory adj wrapper	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L6	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L7	12107	memory with core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L8	252	megacell	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L9	2540	single adj access	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L10	5	megacell same (single adj access)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L11	8	megacell and (single adj access)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L12	12	multistrobe	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:18
L13	32	multi-strobe	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L14	43	multistrobe or multi-strobe	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L15	1	megacell same (multistrobe or multi-strobe)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L16	1	(multistrobe or multi-strobe) same core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L17	3	megacell same lead	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L18	2	(single adj access) adj (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L19	4	(single adj access) with (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L20	4	(single adj access) same (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L21	48	(single adj access) and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L22	40	megacell same core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L23	3	(memory adj wrapper) same (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L24	347023	clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L25	30	(single adj access) with clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L26	1	(memory adj core) and ((single adj access) with clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L27	4	(memory with core) and ((single adj access) with clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L28	15	(memory adj wrapper) and (memory with core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L29	2887	(("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L30	269	(memory with core) and ((("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L31	15	(single adj access) and ((memory with core) and ((("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L32	8	self-timing adj logic	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L33	3	(memory adj core) and (self-timing adj logic)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L34	2619	single adj clock adj cycle	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L35	36	(memory adj core) and (single adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L36	3	"6179489".pn. or "6105119".pn. or "5909559".pn.	USPAT	OR	OFF	2005/11/21 14:19

L37	952	(711/104,105).CCLS.	USPAT; USOCR	OR	OFF	2005/11/21 14:19
L38	74562	burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L39	321	(("711/104,105").CCLS.) and burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L40	15012	internal adj clock$3	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L41	64	((("711/104,105").CCLS.) and burst) and (internal adj clock$3)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L42	534660	core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L43	16	((((("711/104,105").CCLS.) and burst) and (internal adj clock$3)) and core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L44	62761	asynchronous$2	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L45	33	((((("711/104,105").CCLS.) and burst) and (internal adj clock$3)) and asynchronous$2	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L46	12	core and (((((("711/104,105").CCLS.) and burst) and (internal adj clock$3)) and asynchronous$2)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L47	14154	asynchronous$2.ab.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L48	107	burst and (internal adj clock$3) and asynchronous$2.ab.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L49	5	(("711/104,105").CCLS.) and (core and (burst and (internal adj clock$3) and asynchronous$2.ab.))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L50	31	core and (burst and (internal adj clock$3) and asynchronous$2.ab.)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L51	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L52	30	asynchronous$2 with (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L53	11	burst and (asynchronous$2 with (memory adj core))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L54	225	burst and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L55	15	asynchronous$2.ab. and (burst and (memory adj core))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L56	70	(internal adj clock$3) and burst and core and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L57	4	(("711/104,105").CCLS.) and ((internal adj clock$3) and burst and core and (memory adj core))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L58	1943	self-clocking or self-timing	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L59	2887	(("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L60	19	(self-clocking or self-timing) and ((("711/167"). CCLS.) or (("711/169").CCLS.) or (("365/230.02"). CCLS.) or (("365/230.05").CCLS.))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L61	461	asynchronous adj memory	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L62	1	(self-clocking or self-timing) same (asynchronous adj memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L63	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L64	10	(self-clocking or self-timing) same (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L65	8	(self-clocking or self-timing) and (asynchronous adj memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L66	6689	single adj clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L67	77	(self-clocking or self-timing) and (single adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L68	0	(asynchronous adj memory) and ((self-clocking or self-timing) and (single adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L69	8	(memory adj core) and ((self-clocking or self-timing) and (single adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L70	74562	burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L71	101	(single adj clock) same burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L72	1	(memory adj core) and ((single adj clock) same burst)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L73	1	(asynchronous adj memory) and ((single adj clock) same burst)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L74	162925	(memory adj access$3) or (access adj2 memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L75	72	((single adj clock) same burst) and ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L76	277	(single adj clock) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L77	6	(asynchronous adj memory) and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L78	53604	dram	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L79	18	((single adj clock) same ((memory adj access$3) or (access adj2 memory))) same dram	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L80	0	(self-clocking or self-timing) and ((single adj clock) same burst)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L81	101	(single adj clock) and ((single adj clock) same burst)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L82	101	burst and ((single adj clock) and ((single adj clock) same burst))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L83	1	(memory adj core) and (burst and ((single adj clock) and ((single adj clock) same burst)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L84	20	memory adj wrapper	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L85	0	((single adj clock) and ((single adj clock) same burst)) and (memory adj wrapper)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L86	3	(self-clocking or self-timing) and (memory adj wrapper)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L87	1	(self-clocking or self-timing) same (asynchronous adj memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L88	159	(self-clocking or self-timing) and dram	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L89	53	burst and ((self-clocking or self-timing) and dram)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L90	7	(single adj clock) and (burst and ((self-clocking or self-timing) and dram))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L91	42	(asynchronous adj memory) and (single adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L92	64	(self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L93	3	((self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory))) and (single adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L94	25	(memory adj core) and ((self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L95	2619	single adj clock adj cycle	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L96	13	((self-clocking or self-timing) and dram) and (single adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L97	100	((("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.)) and (single adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L98	2	(asynchronous adj memory) and ((((("711/167"). CCLS.) or (("711/169").CCLS.) or (("365/230.02"). CCLS.) or (("365/230.05").CCLS.)) and (single adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L99	1	((self-clocking or self-timing) and dram) and ((((("711/167").CCLS.) or (("711/169").CCLS.) or (("365/230.02").CCLS.) or (("365/230.05").CCLS.)) and (single adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L100	12	((single adj clock) and ((single adj clock) same burst)) and ((((("711/167").CCLS.) or (("711/169"). CCLS.) or (("365/230.02").CCLS.) or (("365/230. 05").CCLS.)) and (single adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L101	40995	dsp or digital adj signal adj processor	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L102	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L103	153	(dsp or digital adj signal adj processor) and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L104	5517	asynchronous with memory	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L105	37	((dsp or digital adj signal adj processor) and (memory adj core)) and (asynchronous with memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L106	74562	burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L107	15	((dsp or digital adj signal adj processor) and (memory adj core)) and burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L108	6689	single adj clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L109	24	((dsp or digital adj signal adj processor) and (memory adj core)) and (single adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L110	38	(memory adj core) same (asynchronous with memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L111	0	each adj clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L112	6689	(single adj clock) or (each adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L113	0	((memory adj core) same (asynchronous with memory)) and ((single adj clock) or (each adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L114	24	(((dsp or digital adj signal adj processor) and (memory adj core)) and (single adj clock)) and ((single adj clock) or (each adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L115	128	(memory adj core) and (asynchronous with memory)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L116	4	((single adj clock) or (each adj clock)) and ((memory adj core) and (asynchronous with memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L117	462	quad adj word	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L118	55	asynchronous same memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L119	0	(quad adj word) and (asynchronous same memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L120	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L121	0	(quad adj word) same (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L122	10	(quad adj word) and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L123	0	(asynchronous same memory adj core) and ((quad adj word) and (memory adj core))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L124	55119	asynchronous	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L125	0	((quad adj word) and (memory adj core)) and asynchronous	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L126	110	(quad adj word) and asynchronous	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L127	0	(memory adj core) and ((quad adj word) and asynchronous)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L128	29137	dsp	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L129	14	((quad adj word) and asynchronous) and dsp	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L130	11500	asynchronous.ab.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L131	7613	one adj clock adj cycle	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L132	189	asynchronous.ab. and (one adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L133	4	(memory adj core) and (asynchronous.ab. and (one adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L134	0	(quad adj word) and (asynchronous.ab. and (one adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L135	23	dsp and (asynchronous.ab. and (one adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L136	64	(self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L137	29137	dsp	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L138	20	((self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory))) and dsp	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L139	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L140	25	((self-clocking or self-timing) same ((memory adj access$3) or (access adj2 memory))) and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L141	1	"5923615".pn.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L142	1	"4799199".PN.	USPAT	OR	OFF	2005/11/21 14:19
L143	570	asynchronous$2 with core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L144	2619	single adj clock adj cycle	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L145	12	(asynchronous$2 with core) and (single adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L146	74562	burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L147	77	(asynchronous$2 with core) and burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L148	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L149	13	((asynchronous$2 with core) and burst) and (memory adj core)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L150	1	"5384745".PN.	USPAT	OR	OFF	2005/11/21 14:19
L151	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L152	1943	self-timing or self-clocking	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L153	74562	burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L154	3	(memory adj core) and (self-timing or self-clocking) and burst	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L155	8	(memory adj core) with (self-timing or self-clocking)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L156	7613	one adj clock adj cycle	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L157	3	(memory adj core) and (self-timing or self-clocking) and (one adj clock adj cycle)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L158	3	(self-timing or self-clocking) and ((memory adj core) and (self-timing or self-clocking) and (one adj clock adj cycle))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L159	30	(single adj access) with clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L160	1	(self-timing or self-clocking) and ((single adj access) with clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L161	1	(memory adj core) and ((single adj access) with clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L162	11	burst and ((single adj access) with clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L163	10559	memory near3 core	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L164	12	self-timing adj logic or self adj timing adj logic	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L165	89453	asynchronous$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L166	8847	single adj clock	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L167	1082	(single adj clock) with (access or read or write or accessing or reading or writing)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L168	7	asynchronous$3 with ((single adj clock) with (access or read or write or accessing or reading or writing))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L169	5	(memory near3 core) and (self-timing adj logic or self adj timing adj logic)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L170	0	(self-timing adj logic or self adj timing adj logic) same asynchronous$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L171	2	(self-timing adj logic or self adj timing adj logic) and asynchronous$3	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L172	1477	711/167.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L173	589	711/169.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L174	558	711/104.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L175	1003	711/105.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L176	694	365/230.02.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L177	924	365/230.05.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L178	3232	365/233.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L179	258	(memory near3 core) and asynchronous$3 and (single adj clock)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L180	8	((memory near3 core) and asynchronous$3 and (single adj clock)) and 365/233.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L181	11	US-5414751-$.DID. OR US-5471607-$.DID. OR US-5699530-$.DID. OR US-5708850-$.DID. OR US-5765218-$.DID. OR US-5781480-$.DID. OR US-5790443-$.DID. OR US-5896543-$.DID. OR US-5923615-$.DID. OR US-5973955-$.DID. OR US-6078527-$.DID.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L182	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L183	277	(single adj clock) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L184	28026	(single adj clock) or (one adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L185	274	(memory adj core) and ((single adj clock) or (one adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L186	24	(memory adj core) same ((single adj clock) or (one adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L187	9697250	@ad<"19981006"	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L188	5	((memory adj core) same ((single adj clock) or (one adj clock))) and @ad<"19981006"	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L189	1037	711/167.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L190	382	711/104.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L191	663	711/105.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L192	514	711/169.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L193	679	365/230.02.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L194	845	365/230.05.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L195	2766	365/233.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L196	6048	711/167.ccls. or 711/104.ccls. or 711/105.ccls. or 711/169.ccls. or 365/230.02.ccls. or 365/230.05. ccls. or 365/233.ccls.	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L197	74	((memory adj core) and ((single adj clock) or (one adj clock))) and (711/167.ccls. or 711/104.ccls. or 711/105.ccls. or 711/169.ccls. or 365/230.02.ccls. or 365/230.05.ccls. or 365/233.ccls.)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L198	23	@ad<"19981006" and (((memory adj core) and ((single adj clock) or (one adj clock))) and (711/167.ccls. or 711/104.ccls. or 711/105.ccls. or 711/169.ccls. or 365/230.02.ccls. or 365/230.05. ccls. or 365/233.ccls.))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L199	6	(memory adj core) and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L200	5	@ad<"19981006" and ((memory adj core) and ((single adj clock) same ((memory adj access$3) or (access adj2 memory))))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L201	1846	memory adj core	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L202	274	((memory adj core) and ((single adj clock) or (one adj clock)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L203	62761	asynchronous$2	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L204	28026	(single adj clock) or (one adj clock)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L205	820	asynchronous$2 same ((single adj clock) or (one adj clock))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L206	22	(((memory adj core) and ((single adj clock) or (one adj clock)))) and (asynchronous$2 same ((single adj clock) or (one adj clock)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L207	9697250	@ad<"19981006"	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L208	15	((((memory adj core) and ((single adj clock) or (one adj clock)))) and (asynchronous$2 same ((single adj clock) or (one adj clock)))) and @ad<"19981006"	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19

L209	277	(single adj clock) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L210	113	asynchronous$2 and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L211	0	(asynchronous$2 and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))) and (self-timing near3 logic)	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L212	24	self-timing near3 logic	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L213	1	"5396608".pn.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L214	6	(memory adj core) and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L215	277	(single adj clock) same ((memory adj access$3) or (access adj2 memory))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L216	113	asynchronous$2 and ((single adj clock) same ((memory adj access$3) or (access adj2 memory)))	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L217	24	self-timing near3 logic	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L218	9697250	@ad<"19981006"	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L219	30	(single adj access) with clock	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L220	0	L215 and L217	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L221	0	L214 and L217	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L222	0	L216 and L217	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L223	1	L217 and L219	USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L224	1495	(711/167).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/21 14:19
L225	588	(711/169).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/21 14:19
L226	602	(365/230.02).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/21 14:19

L227	825	(365/230.05).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/11/21 14:19
L228	3285	L224 or L225 or L226 or L227	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	OFF	2005/11/21 14:19
L229	2	L217 and L228	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:19
L230	1459	711/104,105.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:19
L231	3232	365/233.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:19
L232	4581	L230 or L231	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:19
L233	1	L217 and L232	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/21 14:19
L234	440	711/167.ccls.	US-PGPUB	OR	ON	2005/11/21 14:28
L235	0	186 and 234	US-PGPUB	OR	ON	2005/11/21 14:29
L236	1	169 and 234	US-PGPUB	OR	ON	2005/11/21 14:30
L237	0	96 and 234	US-PGPUB	OR	ON	2005/11/21 14:30
L238	0	218 and 234	US-PGPUB	OR	ON	2005/11/21 14:30

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4. **The impact of delay on the design of branch predictors**
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6. **Issues in partitioning integrated circuits for MCM-D/flip-chip technology**
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